

	Class	Subclass
ISSUE CLASSIFICATION		

PATENT NUMBER

## U.S. UTILITY Patent Application

**O.I.P.E.**

PATENT DATE

SCANNED

Q. A. 2

APPLICATION NO. 09/634068	CONT/PRIOR	CLASS <del>345</del> 732	SUBCLASS <del>339</del> 68	ART UNIT 285 <del>2674</del> 2772	EXAMINER SUAREZ J. CABECA
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# TITLE

Signal transition and stable regions diagram for positioning a logic analyzer sample

PTO-2040  
12/89[illegible]

<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>			<b>CLAIMS ALLOWED</b>	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O. G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.  <input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____  _____  _____	_____ (Assistant Examiner) (Date)  _____ (Primary Examiner) (Date)  _____ (Legal Instruments Examiner) (Date)			<b>NOTICE OF ALLOWANCE MAILED</b>	
				<b>ISSUE FEE</b>	
The terminal _____ months of this patent have been disclaimed.				<b>ISSUE BATCH NUMBER</b>	

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